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10/698,157	10/31/2003	Steven K. Ribling	H0003463	9846

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EXAMINER	
TECKLU, ISAAC TUKU	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/698,157	RIBLING, STEVEN K.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on 10/31/2003.

2. Claims 1-23 have been examined.

Oath/Declaration

3. The office acknowledges receipt of a properly signed oath/declaration filed on 10/31/2003.

Claim Objections

4. Claim 12 is objected to because of the following informalities: claim 12 does not recite its dependence on claim 11. The claim should recite "The architecture of claim 11 wherein ...". Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-5 and 18-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 4 is non-statutory as being "test program architecture" without being supported by hardware such as tangible computer storage or execution engine, which would enable one skill in the art to construe that the compiler is built from tangible product to carry out any functionality being conveyed from the claim. Thus, the compiler is software *per se* and therefore is not being tangibly embodied in a manner as to be executable.

Under the Interim Guidelines Section IV (a) data structures and/or program per se not claimed as embodied in computer-readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional

interrelationships between the data structure and other claimed aspects of the invention which permit the data structure's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory.

Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility (signed 26 October 2005) – OG Cite: 1300 OG 142.

<http://www.uspto.gov/web/offices/com/sol/og/2005/week47/patgupa.htm>

Claims 2-5 are rejected for failing to cure the deficiencies of the above rejected non-statutory claim 23 above.

Claims 18-23 are non-statutory as being "A computer program product " without executable instructions which permit the data structure's functionality to be realized.

Claims 19-23 are rejected for failing to cure the deficiencies of the above rejected non-statutory claim 23 above.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Richardson (US 7,146,572 B2).

Per claim 1, Richardson discloses a data-empowered test program architecture (e.g. FIG. 3 and related text) comprising:

a test executive module (e.g. FIG. 3, element 220 "Test Executive Engine" and related text);

a test framework software module having externally configurable generic software code (e.g. FIG. 3, element 212 and related text) and being coupled for interaction with the test executive software module (col. 6: 60-65 "... test executive software may be operable to receive user input to a GUI ...");

a plurality of software components in a software components module (col. 1: 15-25 "... test modules to test unit under test (UUTs) ...") coupled for interaction with the test framework software module and structured for outputting one or more test reports (col. 1: 15-25 "... the test modules may interact with one or more hardware instruments to test the UUT(s) ..."); and

one or more external control files coupled for configuring the generic software code of the test framework software module (col. 6: 55-65 "... configure a test executive sequence ... various results ...").

Per claim 2, Richardson discloses the architecture of claim 1 wherein the test framework software module further comprises a hardware abstraction interface (e.g. FIG. 3, element 232 and related text).

Per claim 3, Richardson discloses the architecture of claim 1, further comprising an external reuse library having one or more test descriptions of common signal types (e.g. FIG. 3, element 240 and related text) and being coupled for generating the control files (e.g. FIG. 3, element 240 and Sequence Files and related text).

Per claim 4, Richardson discloses the architecture of claim 1 wherein the software components module further comprises one or more software components for interfacing between the one or more external control files and one or more of the test executive software module and the test framework software module (e.g. FIG. 3 and related text).

Per claim 5, Richardson discloses the architecture of claim 1 wherein the software components module further comprises a pass/fail analyzer and report generator having one or more modes of pass/fail analysis and test reporting (col. 1: 25-30 "... pass/fail results ...").

Per claim 6, Richardson discloses a data-empowered test program architecture comprising:

one or more external control files including an external control file having a list of test identification numbers (e.g. FIG. 7, step 353 and related text);

a test executive module having an execution engine coupled to receive one or more test identification numbers from the list of test identification numbers for generating as a function of the one or more test identification numbers a plurality of test actions to be performed on a unit-under-test (e.g. FIG. 3, element 220 "Test Executive Engine" and related text);

a test framework module accessing the plurality of test actions and associated test hardware resources as a function of the test identification numbers, the test framework module (e.g. FIG. 3, element 212 and related text):

i) determining an identification of one of the test hardware resources associated with a current one of the test action (e.g. FIG. 14 and related text),

ii) retrieving the identification of the associated test hardware resource (e.g. FIG. 7, step 351 and related text),

iii) determining a signal type corresponding to the retrieved test hardware resource identification (e.g. FIG. 3, DATA TYPE and related text),

iv) accessing as a function of the signal type one of the external control files having test hardware resource card-type information (col. 23: 45-50), and

v) determining the test hardware resource card-type information as a function of a card-type identifier (e.g. FIG. 15A and related text).

Per claim 7, Richardson discloses the architecture of claim 6 wherein the test hardware resource card-type information includes routing data and parameters for interfacing with an external hardware driver (e.g. FIG. 15A and related text).

Per claim 8, Richardson discloses the architecture of claim 6, further comprising an external reuse library having a plurality of test descriptions corresponding to a plurality of different test signal types (e.g. FIG. 3, DATA TYPE and related text).

Per claim 9, Richardson discloses the architecture of claim 6, further comprising a plurality of software components for interfacing between the external control files and one or more of the test executive module and the test framework module (e.g. FIG. 3, element 232 and related text).

Per claim 10, Richardson discloses the architecture of claim 9 wherein the plurality of software components further comprises one or more modes of pass/fail analysis and test reporting (col. 1: 25-30 "... pass/fail results ...").

Per claim 11, Richardson discloses a data-empowered test program architecture comprising:

means for generating a plurality of test actions to be performed on a unit-under-test; means for accessing the plurality of the test actions (col. 1: 15-25 "... test modules to test unit under test (UUTs) ...");

means for identifying a test hardware resources associated with a current one of the test action (e.g. FIG. 14 and related text); and

means for interfacing with an external hardware driver as a function of identifying the test hardware resources associated with the current one of the test action (e.g. FIG. 3, element 232 and related text).

Per claim 12, Richardson discloses the architecture of claim wherein the means for interfacing with an external hardware driver further comprises:

means for determining a signal type corresponding to the identified test hardware resource (e.g. FIG. 3, DATA TYPE and related text);

means for accessing as a function of the signal type an external control file having test hardware resource card-type information contained therein (col. 23: 45-50); and

means for determining the test hardware resource card-type information as a function of a card-type identifier (e.g. FIG. 15A and related text).

Per claim 13, Richardson discloses the architecture of claim 11 wherein the means for generating a plurality of test actions further comprises means for generating the plurality of test actions as a function of one or more test identification numbers received from a list of test identification numbers (e.g. FIG. 15B and related text).

Per claim 14, Richardson discloses the architecture of claim 11 wherein the means for generating a plurality of test actions to be performed on a unit-under-test further comprises means for generating a plurality of control files for configuring software code for generating the plurality of test actions (e.g. FIG. 3, element 240 and Sequence Files and related text).

Per claim 15, Richardson discloses the architecture of claim 14 wherein the means for generating a plurality of control files further comprises means for generating one or more of the control files as a function of one or more test descriptions of signal types contained in an external reuse library (e.g. FIG. 3 and related text).

Per claim 16, Richardson discloses the architecture of claim 11, further comprising means for performing pass/fail analysis (col. 1: 25-30 "... pass/fail results ...").

Per claim 17, Richardson discloses the architecture of claim 16, further comprising means for generating one or more test reports.

Per claim 18, this is the computer program product version of the claimed architecture discussed above (Claim 11), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 19, this is the computer program product version of the claimed architecture discussed above (Claim 12), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 20, this is the computer program product version of the claimed architecture discussed above (Claim 13), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 21, this is the computer program product version of the claimed architecture discussed above (Claim 16), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 22, this is the computer program product version of the claimed architecture discussed above (Claim 17), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Per claim 23, this is the computer program product version of the claimed architecture discussed above (Claim 14), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Richardson.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER